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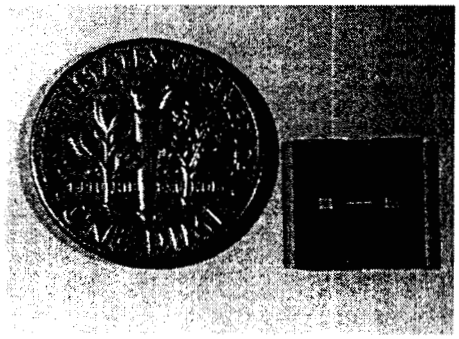
Juergen Mueller, Steven Vargo, Indrani Chakraborty, John Forgrave, David Bame, and William Tang

Jet Propulsion Laboratory
California Institute of Technology
Pasadena CA 91109



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The Micro-Isolation Valve: Introduction of Concept and Preliminary Results

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A feasibility investigation for a newly proposed microfabricated, normally-closed isolation valve was initiated. The micro-isolation valve is silicon based and relies on the principle of melting a doped plug, opening an otherwise sealed flow passage. This valve may thus serve a similar role as a conventional pyrovalve and is intended for use in micropropulsion systems onboard future microspacecraft, having wet masses of no more than 10-20 kg, as well as in larger scale propulsion systems having only low flow rate requirements, such as ion propulsion or Hall thruster systems. Two key feasibility issues - melting of the plug and pressure handling capability - were addressed. Thermal finite element modeling showed that valves with plugs having widths between 10 and 50 μm have power requirements of only 10 - 30 Watts to open over a duration of 0.5 ms or less. Valve chips featuring 50 micron plugs were burst pressure tested and reached maximum pressure values of 2850 psig (19.4 Mpa).

I. INTRODUCTION

Strong recent interest within the aerospace community to built smaller spacecraft necessitates the development of space hardware able to fit the unique requirements with respect to mass, size, and power. These requirements may be quite as indicated by recent research and development work performed on microspacecraft designs within the National Aeronautics and Space Administration (NASA)[1,2]. Microspacecraft are expected to have masses of 10-20 kg and less and power availabilities of only a few tens of Watts. This dramatic decrease in weight, size and available power levels will thus require radically new approaches in the design of spacecraft components.

Several activities are underway in the propulsion field to address these issues[2]. At the Jet Propulsion Laboratory, for example, work is being performed on a small liquid-fed attitude control thruster[s3,4], micro-ion engine technologies[5-7], as well as some initial work on valves. Improvements in valve technolgies with respect to mass, size and power are crucial to the success of micropropulsion technologies since it is important to ensure that the entire propulsion system weight is reduced, which includes its feed system components.

In this paper we will discuss a newly proposed, normally closed isolation valve concept which is based in its fabrication on MEMS (Microelectromechanical Systems) technologies. MEMS technologies have recently gained increased attention in microspacecraft designs due to their significant potential for miniaturization. While more traditional "machine-shop" technologies have shown impressing decreases in component mass and size reductions[8], MEMS components offer the vision of a highly integrated, extremely small propulsion system by bonding MEMS-based valve components directly to MEMS-based thruster components to form extremely tightly configured "feed-system-on-a-chip" modules.

Currently available MEMS valve technology, as provided by the non-aerospace industry, however, does not appear applicable to in-space use for a variety of reasons, foremost among them being concerns regarding leakage. The micro-isolation valve proposed here could potentially provide essentially zero-leakage rates prior to opening of the valve, thus simulating the conventional pyro-valve technology used in macro-propulsion systems. While initially targeted for micropacecraft use, applications of the micro-isolation valve may also be found in more conventionally sized propulsion systems requiring only low flow rates, compatible with the to be expected small flow dimensions that could be provided on a chip. Such criteria may be fulfilled by certain electric propulsion systems, such as ion and Hall thruster systems.

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*Advanced Propulsion Technology Group, Senior Member AIAA
**MEMS Group, Micro Devices Laboratory
+Reliability Engineering Group
++Propulsion Flight Systems Group
#Group Supervisor, MEMS Group, Micro Devices Laboratory

In the following sections the micro-isolation valve concept will be introduced, key feasibility issues will be identified, and initial tests and analysis aimed at addressing these issues will be discussed.

II. MICRO-ISOLATION VALVE CONCEPT AND FEASIBILITY ISSUES

Concept

The micro-isolation valve relies on the principle of melting a doped silicon plug, which in the valve's normally closed position blocks the flow passage. Plug melting will be achieved by passing an electric current through it and resistively heating it. The valve will thus serve a similar function as a normally-closed pyrovalve, providing an essentially zero leak rate prior to actuation by completely sealing the flow passage. Unlike a pyrovalve, however, the here proposed valve type will not rely on pyrotechnic actuation, thus avoiding the potential for pyroshocks as well as simplifying valve integration.

A schematic of the valve can be seen in Fig. 1. The valve is micromachined and silicon-based. It consists of two basic components: the silicon chip featuring all the flow passages and inlet and outlet, and a Pyrex cover to seal the flow passages while allowing to view the internal of the chip. Later versions may be entirely assembled from silicon. The silicon-Pyrex bond is achieved by means of anodic bonding, a standard bonding technique in the microfabrication field by which silicon and a special grade of Pyrex (Dow Corning 7740) are placed in immediate contact with each other. Applying pressure and an electrostatic potential across the bond surface at a temperature of approximately 450 C causes the two chips to fuse together. The bonding mechanism is believed to be due to the formation of a thin silicon oxide layer along the bond surface and is thus chemical in nature. Very strong bond strengths can be obtained as will be seen below.

The silicon side of the chip features the plug, the valve-internal flow channels and the filter, and will be batch-fabricated from larger silicon wafers using microfabrication techniques. Propellant entering the valve chip will flow through a short channel section etched into the silicon side of the chip until it reaches the plug. Channels in the chip are fabricated using deep trench reactive ion etching (RIE) techniques. This etching process is highly directional and allows deep features to be etched into the chip with very straight wall sections up to aspect ratios of 30:1.

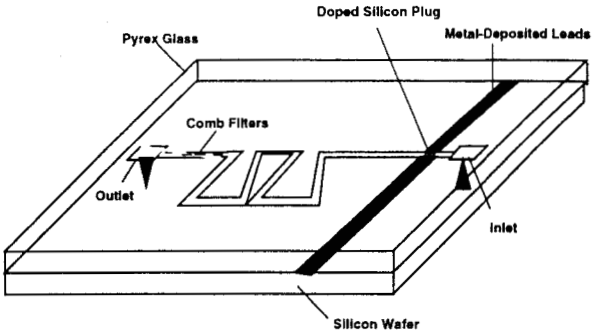

Fig. 1: Schematic of the Micro-Isolation Valve Concept

Metal (gold) leads deposited onto the silicon substrate and partly overlapping the doped-silicon plug region connect the plug to an external valve-opening circuitry. Passing an electrical current through the plug will melt and/or vaporize the doped silicon and propellant located upstream of the valve inlet will push the plug debris downstream, thus opening the valve. Beyond the plug location the flow path continues. In order to prevent plug debris from contaminating flow components located downstream of the isolation valve, potentially clogging lines, contaminating valve seats or otherwise interfering with the proper function of those components, it is crucial to trap the debris within designated, non-critical regions of the valve without re-closing the flow path again. Figure 1 shows one potential flow path configuration designed to accomplish this task. Here, the flow path goes through a series of S-shaped turns designed to trap molten plug debris in the corners of the etched channel. Oversizing the channel, in particular near the corners, will avoid clogging. Other configurations may be explored as the experimental program progresses, such as parallel flow passages for redundancy, for example. A comb filter integrated in the flow path downstream of the S-shaped condensation region will serve to trap solidified debris that may not have been condensed at the flow path walls. The comb filter features a staggered filtration design, consisting of several rows of silicon posts. The spacing between posts decreases for rows located further downstream, allowing larger particles to be trapped by upstream rows with wider post spacings and smaller particles by rows with narrower post spacings located further downstream, thus avoiding clogging of the filter. using MEMS-based techniques, it is expected that very small filter ratings may be produced, into the μm-range.

Key Feasibility Issues

Several key feasibility issues can immediately be identified for this valve and will need to be addressed in the research program. Among these issues are:

(1) *Plug Melting*: Melting of the plug will need to be demonstrated. Power levels should not be excessive in order to be compatible with microspacecraft power requirements, although energy storage devices, such as capacitors, may be used to relax this requirement. Melting should also be achieved quickly to limit heat conduction losses to the remainder of the chip where high temperatures could lead to thermal stresses, in particular between bonded components that feature a coefficient of thermal expansion (CTE) mismatch. In the case of the discussed laboratory devices this mismatch may occur between silicon and Pyrex, in particular above temperatures of about 300 C where the CTE values of Dow Corning 7740 Pyrex and silicon begin to diverge. Even in the case of future, all-silicon version, of this valve mismatches may still occur between the valve and packaging.

(2) *Pressure Handling Capabilities:* The micro-isolation valve chip will be required to maintain large internal pressures in particular in the case of gaseous propellant applications, such as some electric propulsion systems. Typical gas storage pressure in a xenon feed system are around 2000 psi (13.6 MPa). Since factors of safety of 1.5 are typically required, burst pressure may have to be as high as 3000 psi (20.4 MPa). This poses a major design challenge given that the chip consists of silicon and glass. Of particular interest in this context is also the plug. Thermal considerations, alluded to above, will drive the plug dimensions to smaller widths in order to minimize power requirements for melting. Pressure requirements, on the other hand, will drive the plug design into the opposite direction.

(3) *Contamination Related Issues:* Trapping of plug debris inside the micro-isolation valve chip will have to be demonstrated. No debris can be allowed to propagate downstream into other flow components, in particular not onto valve seats that may be located downstream of the isolation valve. For micropropulsion applications in particular, these valve seats may themselves be very small in size, thus resulting in tight filter ratings requirements. In principle, micro-machined comb filter approaches may offer a solution in this regard, thus, isolation valve integrated filter designs will need to be explored.

As will be shown in the remainder of this paper, both items (1) and (2) have been addressed so far and show promising results. Contamination and filtration issues will be considered at a later stage further into the program. In the following sections we will discuss thermal finite element modeling of valve plug designs, allowing initial estimates of power requirements and valve actuation times, as well as burst pressure test results for the chip.

III. THERMAL MODELING OF PLUG DESIGNS

In order to determine an appropriate valve plug design, the plug region of the valve was modeled thermally using a finite element package. The Finite Element Analysis (FEA) software used was PATRAN 6.0. The model of the plug region of the valve contained about 10,000 elements. In order to conserve computation time, only a quarter section of the plug, cut along two lines of symmetry, was modeled. In line with test chip design and fabrication considerations, the plug dimensions were chosen as 300 by 300 μm^2, and two plug thicknesses, 10 μm and 50 μm, were considered. The thinner plug barrier will represent a thermally favored design, since melting this barrier will be easier to accomplish, while the thicker barrier, as will be seen in Section IV, will be favored based on pressure handling considerations.

Heating of the plug will occur resistively by passing an electric current through it. Since silicon is a semiconductor, it will be doped to increase its electric conductance. Fabrication constraints are such that doping can only be achieved up to certain depths into the silicon due to diffusion limitations. Even using ion implantation with a combined thermal drive-in, thicknesses of more than 10 μm can usually not be achieved. In the fabrication of the micro-isolation valve we are therefore considering wafers that feature epitaxially grown doped silicon layers. These layers may be grown to thicknesses up to about 40 μm. Currently we have access to wafers featuring a 25 μm thick doped silicon epi layer. Thus, in the calculations it is assumed that heat is deposited into the barrier only over a thickness of 25 μm, as measured from the top of the barrier.

All calculations were performed for a normalized 1W total heater input power. Since this model relies entirely on heat conduction, and the equations for conduction are linear with power, temperature values can easily be extrapolated to other power levels. Test cases with this model were run to confirm this approach.

Figure 2 shows the case of a 10 μm thick plug (barrier) wall, as represented in this quarter section of the plug area. This section was obtained by both cutting the channel length-wise along its center line, and, in a perpendicular direction to the previous cut, dicing the barrier along its center plane. The part of the section extending above the height of the barrier wall in Fig. 2,

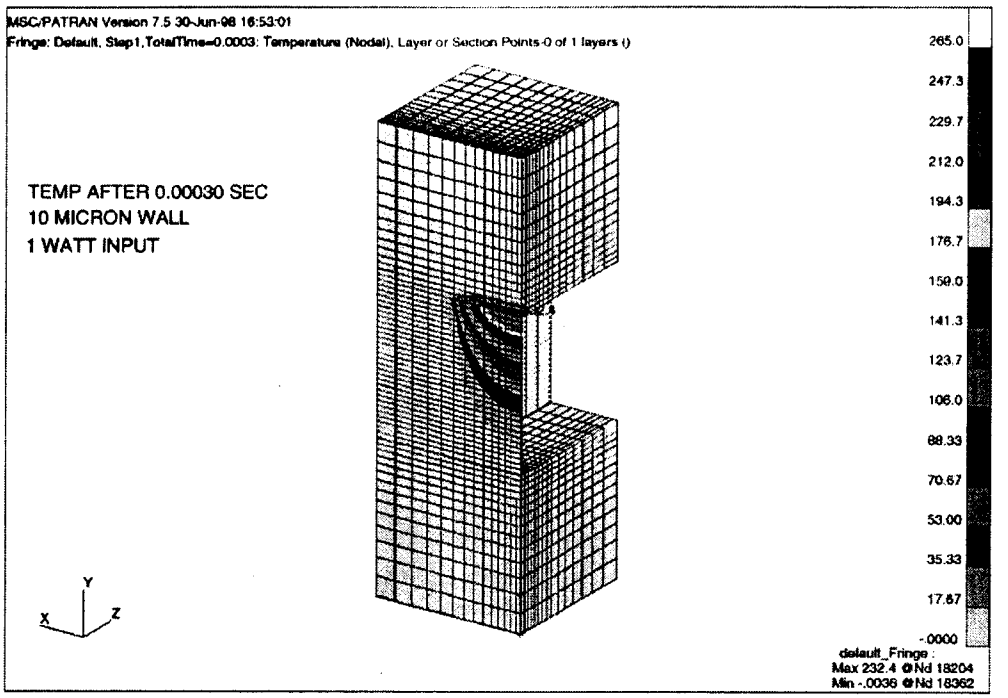

Fig. 2: Results of Thermal Modeling of Plug Quarter Section for a 10 μm Plug Thickness

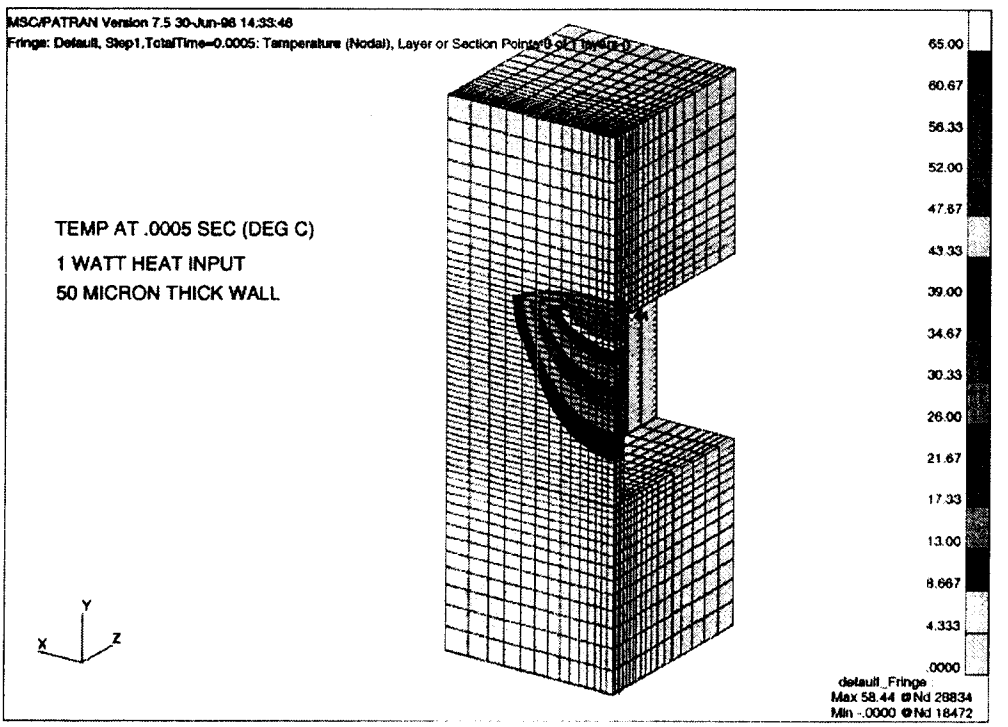

Fig.3: Results of Thermal Modeling of a Plug Quarter Section for a 50 μm Plug Thickness

i.e. the upper third of the section, represents the Pyrex cover. The lower two-thirds of the section represent the silicon wafer. The flow channel can be seen extending behind the plug. Thus, as represented in Fig. 2, only half the width and half the thickness of the barrier is shown and of the channel extending behind the barrier only one half is shown as well. Propellant would thus either flow into or out of the plane of the paper, if the barrier was open, depending on flow direction.

As can be seen by inspecting Fig. 2, the peak temperature in this 1-W case reaches a value of 232 C in the center of the barrier near its top, where it bonds to the Pyrex, after only 0.3 ms. Thus, for a case of 10 W input power, which even without energy storage devices is not an unreasonable power level for a microspacecraft application , this temperature would be as high as 2320 C. Silicon melts at 1400 C. Thus, for a 10 W case, a substantial fraction of the barrier, approximately representing the upper 20% of the barrier, would reach melting temperatures, as can be seen by following the temperature contours in Fig.2.

These considerations do of course not take into account any influence the propellant pressure may exert on the barrier. It is conceivable that due to softening of the silicon barrier prior to melting, and the application of pressure onto barrier, even regions of the barrier which are below the actual melting point may break and be opened up. On the other hand, as the barrier starts to heat from the top where the electric current is flowing, the top 25 μm, upon reaching melting temperature, may be removed, thus loosing the ability to add further heat since current cannot be conducted below this depth due to the lack of doping. These considerations thus emphasize the importance of obtaining as thick a doped epi-layer as possible. As mentioned above, about 40 μm is currently achievable.

While it may not be possible to remove the barrier in its entirety, an orifice of about 25 - 40 μm in depth and of a comparative or larger width appears sufficient to allow for sufficient flow rates even for liquid propellants at very little pressure drops, as was found out in related micropropulsion experiments recently conducted and discussed in a companion paper[4]. In that experiment, a vaporizing liquid micro-thruster chip featuring a 100 x 100 μm^2 inlet and a 50 x 50 μm^2 outlet, separated by a channel of similar dimensions and length as the one considered for the micro-isolation valve, showed no problems in passing appreciable amounts of fluids (water) at feed pressures of 5 psi and less. The flow channel dimensions in the micro-isolation valve will continue to be kept larger than the expected orifice in the barrier to reduce pressure drops inside the chip and to help avoid clogging of flow passages, in particular downstream of the plug region.

Figure 3 shows the case of a plug of 50 μm thickness. Calculations were again performed in the normalized case of 1 W power consumption. After an on-time of 0.5 ms, comparable to the previously discussed 10 μm plug case, peak temperatures reached a value of about 58 C. Thus, in order to reach at least 1400 C in a comparable time period, approximately 1400/58.6 * 1 W = 24 W of power would be required over the duration of 0.5 ms. These power requirements are still very benign and may still not require dedicated energy storage devices (capacitor banks) for the valve as power levels of that magnitude may be available on a 10-20 kg microspacecraft[2]. Given that the peak temperature shown in Fig. 3 is only reached at one location just below the top of the barrier, slightly higher power levels will likely be required in practice to heat the barrier to melting temperature to a depth of 25 - 40 μm, depending on doping thickness. Using the plot in Fig. 3, for a melting temperature of 1400 C to a depth of 25 μm one may estimate a power requirement of about 28 W over a duration of 0.5 ms. A similar extrapolation performed using the temperature plot in Fig. 2 for the 10 μm barrier results in a power estimate of about 7 W for a duration of 0.3 ms to open the valve to a depth of 25 μm.

Thus the thermal analysis performed here clearly seems to indicate that valve actuation is feasible with reasonable power/energy requirements expected to be available on microspacecraft. Should power requirements be larger in practice, the possibility always exists to provide dedicated energy storage devices (capacitors) to, temporarily over the short duration required to actuate the valve, boost the power levels for the valve. The aforementioned numerical results obviously will need to be verified through experiments and such experiments are scheduled immediately after completion of burst pressure tests to be discussed next.

IV. BURST PRESSURE TESTS

Test Chip Design

As was mentioned in Section II, valve plug design, among other things, will be governed by two predominant, yet conflicting, requirements. Thermal considerations, as discussed above, will favor a thin plug design to reduce power requirements to melt the barrier. Requirements with respect to pressure handling capability, on the other hand, may drive the design to larger plug thicknesses. In order to finalize the plug

design, a series of tests was thus conducted to determine burst pressures for different plug thicknesses and valve body configurations. An experimental, rather than a numerical, approach was chosen in the evaluation of the pressure handling capability of the valve chips due to the to be expected statistical variation inherent in such tests, possibly depending on small material defects or bond strengths of the anodic bonds, in particular along the top of the barrier, which would have been difficult to predict and model accurately.

In order to perform these tests, a series of dedicated test chips were fabricated. One of these chips is shown in Fig. 4 and a schematic outlining some of its design features is depicted in Fig. 5. This chip design will be referred to as "Batch-1" in the remainder of this paper. The chip design focuses solely on the plug region and the optimization of the plug design. Besides being used for burst pressure tests in this test run, it will also be used in plug vaporization tests. The chip features a straight, 4 m long channel section with a cross section of 300 x 300 μm^2. The plug is located in the center of the chip, dividing the channel section in two halves. Several different plug designs were tested, ranging in thicknesses from 10 μm to 100 μm. The channel is connected to inlet and outlet through which gas can enter and exit the chip from the bottom surface. The chip is sealed with an anodically bonded Pyrex cover. This seal necessitates the fabrication of two recesses into the chip which feature the electric leads to the plug, visible as the lightly-colored rectangular regions in Fig. 4. Since metal deposition may be as thick as several tenths of a micron, depositing the metal lead directly onto the un-recessed surface would have led to leakage paths immediately adjacent to the metal deposits, as the Pyrex would have been forced to bent over them.

Although doping of the silicon is possible to provide electric contacts, its resistivity is higher than that of gold, and since the desire was to create the majority of the resistance drop in the plug region were heating was supposed to occur, gold was chosen. Immediately adjacent to the plug the silicon is doped to make it electrically conductive. The metal leads partially overlap with these doped regions to make electric contact with the plug. The chip itself can then be electrically contacted near the edges, were notches in the Pyrex (see Fig. 4) are provided for this purpose. Contacting the chip near its edges is preferred as it minimizes the wire length needed for wire bonding. These wires are typically very thin and fragile and minimizing their lengths simplifies handling of the chip.

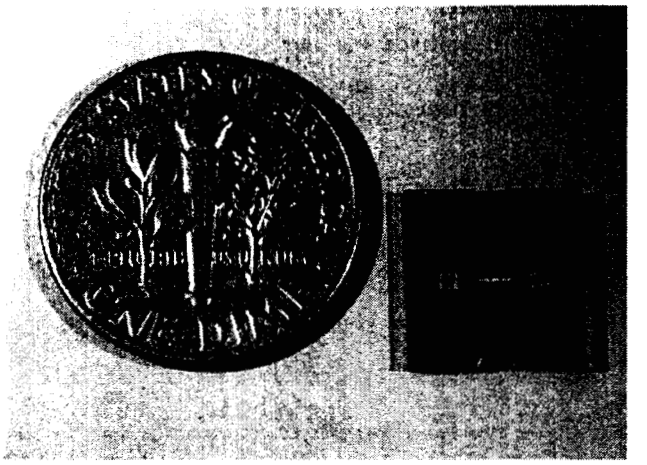

Fig. 4: Micro-Isolation Valve Test Chip

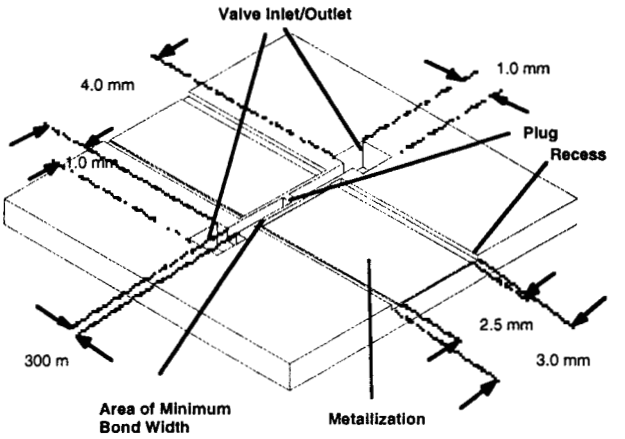

Fig. 5: Schematic of "Batch-1" Type Test Chip

No current input was needed for the burst tests. However, since the recess may impact pressure handling capability, it was integrated even into the chips for burst testing. The reason for this decision may be seen in Fig. 5 and also in Fig.6. Due to the recess, there exist regions of minimal bond width between the channel and the recess across which debonding and leakage may occur at very high internal pressures. As will be seen below, this did indeed occur at pressures exceeding 1800 psi (12.2 MPa), thus below the design goal of about 3000 psi (20.4 Mpa) as dictated by electric propulsion feed system requirements as discussed above. For this reason a second chip design was also tested.

This second batch of chips, referred to from here on as "Batch-2", is shown in a schematic depicted in Fig. 7. This design features narrowed recess regions (only 1.5 mm in width) which tapered to an even smaller width (0.75 mm) immediately before reaching the plug region.

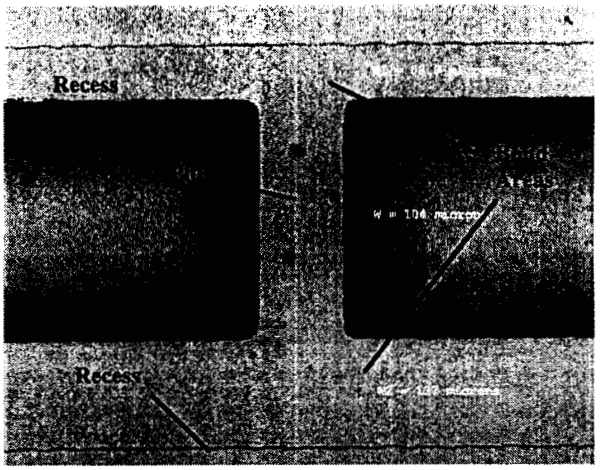

Fig. 6: Close-Up of Plug ("Batch-1" Chip#12)

This increased the overall silicon/Pyrex bond area. Another new design feature was added to this chip. Wrapping around the recess area and the entire channel section is a narrow, 25 μm wide trench, as can also be seen in Fig. 8. This trench serves as an electrical insulation: As was pointed out in Section III, in order to create a large enough opening in the barrier, the silicon surface has to be doped to a sufficient depth. More conventional doping techniques such as ion implantation followed by a thermal drive-in, could only provide sufficient doping to a depth of about 10 μm.

However, using the described doped epi-wafer technique, doped silicon regions as thick as 40 μm may be grown on a silicon substrate wafer. In this case, however, the entire chip surface is doped, and not merely the plug region. This could allow current to flow around the channel section to the opposite metal lead, rather than having to force its way through the high-resistivity plug region. To create a high resistivity path for the current around the channel section, the trench narrows the region along which current may flow to 200 μm, which is the separation between the isolation trench and the channel. (Obviously the trench may not intersect with the channel as a leakage path would be created through the trench). Again, for burst testing, since no current flow was intended, this design feature would not have been needed. However, since it may impact pressure handling capability as it locally decreases bond widths, this design feature was included in the burst tests.

Chip Fabrication

The fabrication of the micro-isolation valve is a combination of silicon etching and wafer bonding techniques. Desired features are first etched in silicon to create the device's structure and then the chip is pressure

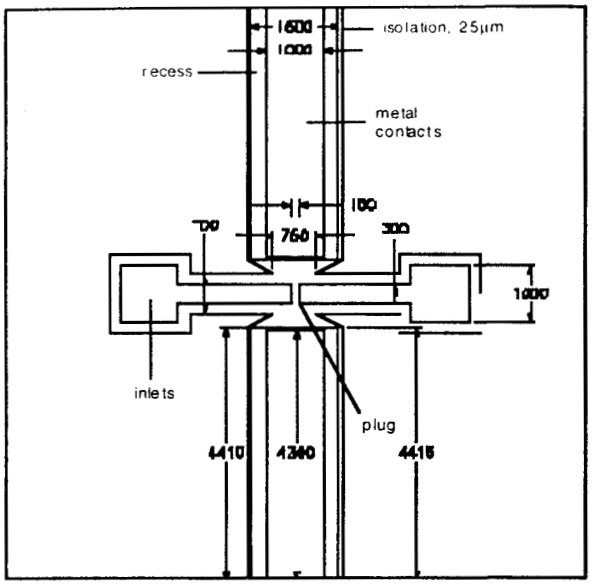

Fig. 7: Sketch of "Batch-2" Type Test Chip

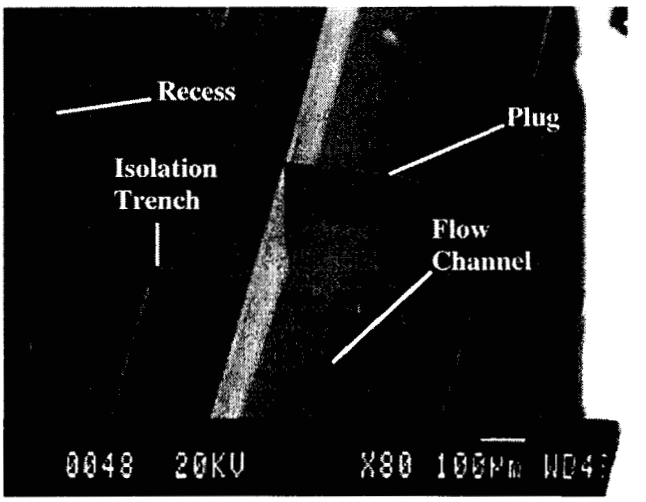

Fig. 8: Close-Up of Plug Area ("Batch-2"-chip) with Recess and Isolation Trench

sealed via anodically bonding a Pyrex wafer to the silicon. Etching of silicon is achieved using a leading-edge deep Reactive Ion Etching (RIE) system available at JPL's Micro Devices Laboratory (MDL). This deep RIE system, which is manufactured by Surface Technology Systems, Inc. (STS), provides highly anisotropic etching parameters in silicon. The fabrication of these structures results from the utilization of an alternating inductively coupled plasma of SF_6 and C_4F_8 gases[9]. Etching of exposed silicon areas occurs during the SF_6 plasma step where a fluorine-rich environment chemically reacts with and removes silicon from the wafer. The C_4F_8 step in the etching process is used to control the anisotropy of the etching by passivating the sidewalls of the etched features. This steps helps to prevent lateral etching (i.e.

undercutting) of the silicon features as well as the mask layer during the next etch step. The STS system can provide silicon etching rates of about 4.5 μm/min, aspect ratios of 30:1 and sidewall angles of 90±<0.25°. The following RIE etching process steps are needed for creating the micro-isolation valve structure: recess etch (etches a 1.5 μm recess for metal contact strips), front-side etch (etches the electrical isolation, inlet/outlet and channel 300 μm deep, i.e. half the wafer depth) and back-side etch (etches the inlet/outlet 300 μm deep). The 300 μm back-side etch completes the micro-isolation valve structure.

Burst Test Set-up and Procedure

The burst test set-up is shown in Fig. 9. The chip was bonded to a stainless steel fixture, connecting the inlet and outlet holes of the chip to two tube stubs featuring Swagelok® fittings. One fitting was connected to the pressurant supply while the other was connected to a leak detector, thus allowing for valve internal leak checks across the plug. External leaks were monitored by determining the pressure decay in the system, i.e. if no internal leak could be registered with the leak detector, yet pressure decayed, the leak was determined to be external. The entire chip assembly is placed into a test barricade for protection during burst tests. The pressurant supply provides regulated helium pressure to the valve inlet. Pressure is measured with a 0-5000 psig pressure gage mounted directly upstream of the chip to an accuracy of ± 0.25%.

The test procedure begins with a slow purge and vent of the entire upstream pressurant system (up to the valve chip plug) to fill the system with helium. The pressure is then slowly increased in 100 psig steps and held at those increment levels to check for external (through pressure decay) and internal leaks across the chip barrier (with the leak detector).

Results - "Batch-1" Type Chips

Results obtained for Batch-1 type chips are summarized in Table 1. This table lists a chip identification number, the burst pressure or the pressure at which leakage (external or internal) occurred, the mode of failure (external leak, internal leak or burst), the plug width and the bond widths to both sides of the channel, formed by the boundaries of the channel and recess, respectively (compare with Fig. 6). Although intended to be equal, a slight misalignment of masks caused the bond

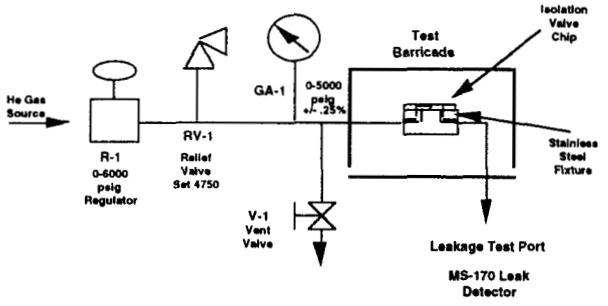

Fig. 9: Burst/Leak Test Set-up

width to one side of the channel to be bigger than the one on the opposite side. All the chip dimensions were measured under an electron microscope. This was possible, as will be seen below, because the Pyrex cover glass blew off the silicon side of the chip at the time of failure. In the cases were this did not occur (Chips # 2 and # 6), this was not possible since Pyrex is not transparent when observed under an electron microscope. Thus the nominal plug widths were listed in Table 1 for these chips instead.

As can be seen, chips featuring 10 μm wide plugs suffered from internal leakage. Inspection of the chips after the test showed that the bond between the top of the barrier and the Pyrex had failed. Good anodic bonds to very thin structures had been noted before by the authors to be difficult to achieve and one of the goals of this test was to study the integrity of these thin bonds. Chips with somewhat larger bond widths (27 and 38.8 μm) performed better, however, burst failure of the chip occurred at comparatively low pressures of 1050 psig (7.4 MPa) and 900 psig (6.1 MPa). In the case of Chip #13, the bond widths next to the channel were rather small when compared to the other chips, with a minimum bond width of only 22.5 μm. On the other hand, chips with thicker plug widths and larger bond widths along the channel walls performed better, reaching burst pressures as high as 1850 psig (12.6 MPa).

The burst failure mechanism for these chips was always the same and can be inspected in Fig. 10. The particular chip shown in this Figure is Chip #12. As can be seen, that portion of the Pyrex covering the inlet side of the chip blew off. It thus was clear that the anodic bond between the silicon and Pyrex had failed. Consequently, a redesign of the chip was pursued, leading to the "Batch-2" design described above, featuring larger bond widths. Results are described below.

Table 1: Burst/Leak test Data for "Batch-1" Type Chips

Chip I.D.	Burst Pressure (psig)	Leak/Burst Mode	Plug Width (μm)	Sidewall Bond Widths (μm)
1	1050	burst, no leak prior	27.1	111/69.1
2	250	internal leak	10 nominal	
3	1650	burst, no leak prior	58.9	78/124
6	100	internal leak	10 nominal	
8	1750	burst, no leak prior	100	122/64.1
12	1850	burst, no leak prior	104	68.8/137
13	900	burst, no leak prior	38.8	22.5/68.3

Results - "Batch-2" Type Chips

Six "Batch-2" type chips were tested featuring plug widths of 20, 25 and 50 μm. All chips with plug widths below 50 μm failed due to internal leaks. This result did not come unexpected since it was noted during the first fabrication run for these chips that the plug barriers were thinning toward the bottom of the channel to inappropriate etching parameters in the RIE etching process. Thus, breakage of the barrier was the likely cause for this internal leakage, however, post-test inspections are still on-going. This issue of barrier thinning was resolved in the latest fabrication run and new chips feature almost perfectly straight walls. testing of these chips is scheduled to begin shortly.

The chips featuring thicker plugs (50 μm), on the other hand, performed very well. Two of these chips were tested and burst pressures of 2825 psig (19.2 Mpa) and 2850 psig (19.4 MPa) , respectively, were recorded. These values can be considered as quite remarkable, considering that the valve chip is fabricated entirely from silicon and glass. Both pressure values approach very closely the desired burst pressure value of 3000 psig (20.4 MPa), at which point this valve would be able to withstand, at a margin of safety of 50%, propellant storage pressures found in xenon feed systems.

The failure mode at burst for these "Batch-2" type chips also changed, as can be seen by inspecting Fig. 11. Here, a piece of Pyrex located directly above the inlet hole was blown out, however, the Pyrex did not detach from the silicon substrate, as was observed for "Batch-1" type chips. Thus, it appears that Pyrex failure, rather than bond failure, was the cause for the burst of this type of chips. Therefore, the increased bond area between the Pyrex and silicon substrate in the "Batch-2" type chips appears to have served its purpose of increasing overall bond strengths. It thus seems possible that busrt pressures for this valve could easily be extended to even higher pressures through the use of thicker Pyrex. Current Pyrex thickness is 0.5 mm. Further testing with this type of chip, featuring thicker Pyrex as well as the improved thinner barrier designs, will be performed,

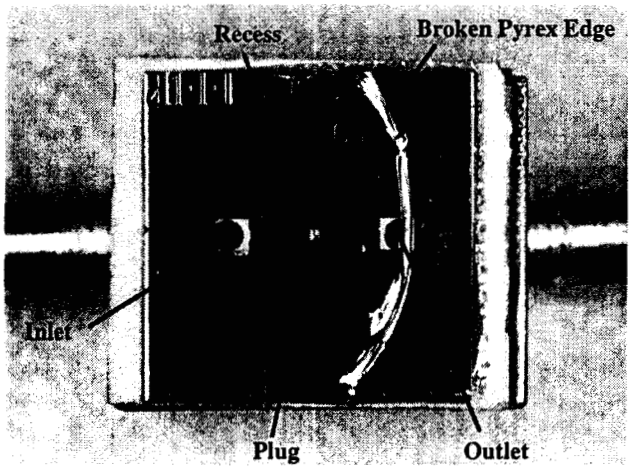

Fig. 10: Post-Test Image of Burst "Batch-1" Type Chip. Notice Pyrex Blown Off.

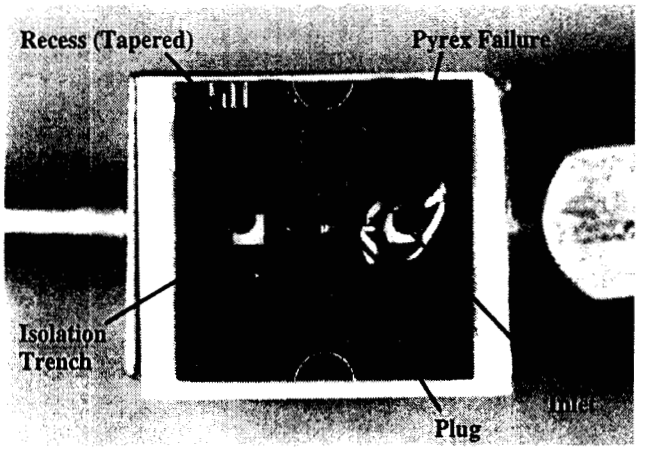

Fig. 11: Post-Test Image of Burst "Batch-2" Type Chip. Notice Hole in Pyrex over Inlet.

followed by plug vaporization tests of the appropriate plug designs.

V. CONCLUSIONS AND FUTURE WORK

Development of a newly proposed microfabricated, normally-closed isolation valve design was initiated. This valve relies on the melting of a doped silicon plug to open an otherwise sealed flow passage. Applications for this device may be found in micropropulsion feed systems, such as those envisioned for microspacecraft in the 10 - 20 kg class and below, or for larger propulsion feed system as well where only low flow rates may have to be maintained, such as some of the electric propulsion systems (ion and Hall thruster). The micro-isolation valve would thus play the role of a normally-closed pyrovalve in conventional systems, however, do not rely on pyrotechnic actuation.

Several key feasibility issues need to be addressed in the valve evaluation, such as investigating the ability to melt a silicon plug at power levels acceptable in a microspacecraft environment, the ability to maintain high valve internal pressures of at least 3000 psi (20.4 MPa) to be of use to the aforementioned electric propulsion systems, as well as trapping of plug debris inside the chip through adequate filtration schemes. In the current study, both plug melting as well as pressure handling abilities of the valve were addressed. Both investigations are inter-related with respect to the plug design. Thermal considerations alone would lead to thinner plug widths, since thinner plugs will be easier to melt, whereas pressure handling considerations will drive the design to thicker plugs. Both issues were therefore addressed simultaneously. Filtration related investigations will follow as this program progresses.

Thermal finite element modeling indicates that plugs of thicknesses between 10 - 50 μm can be melted at power levels ranging between approximately 10 - 30 Watt if applied over a duration of approximately 0.5 ms. These numerical values are very encouraging as they indicate that power requirements are not excessive, even fitting some of the forecasted microspacecraft power constraints. Since power levels have to be applied only over very short time durations, energy storage devices, such as capacitors, dedicated to the valve opening sequence could easily be envisioned for microspacecraft with lower onboard power levels.

Burst pressure tests of several valve test chips were performed to determine pressure handling capabilities. Dedicated test chips were designed aimed at specifically investigating the critical plug region of the valve. Different plug widths and chip designs were investigated. Building on earlier tests, the final design reached burst pressure values as high as 2850 psig. Pyrex breakage was determined as the failure mechanism. Pyrex-to-silicon anodic bonds, on the other hand, were able to withstand even these high pressures. Given the fact that the entire valve is fabricated from silicon and Pyrex glass, these obtained high burst pressure values are quite remarkable, however, could be reproduced. It is felt that using a thicker Pyrex, or, in later experiments not requiring visual access to the chip, silicon material, even higher burst pressure may be attained.

Future work will include further burst pressure testing, in particular extending testing to newly fabricated chips featuring plug widths of less than 50 μm which had failed in previous tests likely due to thinning of the plug barrier near the bottom of the flow channel, a result of processing difficulties. Following these tests, plug melting experiments will be performed to verify thermal calculations performed in this study. Finally, with a selected optimal plug design, filtration tests will be conducted.

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